2.5 - 6.0 GHz BROADBAND GaAs MMIC VCO

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ABSTRACT

This paper describes the design, analysis, and experimental results of a GaAs MMIC VCO which continuously tunes from 2.5 to 6.0 GHz.

INTRODUCTION

Broadband FET voltage controlled oscillators are typically designed using the topology shown in Figure 1. Positive feedback is created by forcing the drain current into the gate by presenting a high reactance on the source using a capacitance. A resonance condition is established by placing an inductance in the gate. Tuning is achieved by replacing the source capacitance with a varactor and by placing a varactor in series with the gate inductor. This particular topology has been proven successful in a 2-4 GHz MMIC VCO [1] using on-chip integrated varactors.

In order to achieve maximum bandwidth it is necessary to use off-chip discrete hyperabrupt varactors which have significantly higher capacitance ratio than currently available on-chip varactors. A VCO circuit can be optimized for maximum bandwidth using computer-aided design techniques and implemented using an MMIC realization which offers reduced parasitics and optimized device selection.

DESIGN ANALYSIS

Several different VCO topologies were analyzed for maximum bandwidth using GaAs hyperabrupt varactor models with a capacitance ratio of 12:1. Three VCO topologies were analyzed by changing the positive feedback mechanism as shown in Figure 2 with the following results:

Feedback Type	Percent bandwidth
Circuit A (basic configuration)	47%
Circuit B	81%
Circuit C	85%

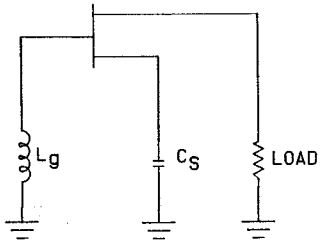

Figure 1. Typical Broadband VCO Topology.

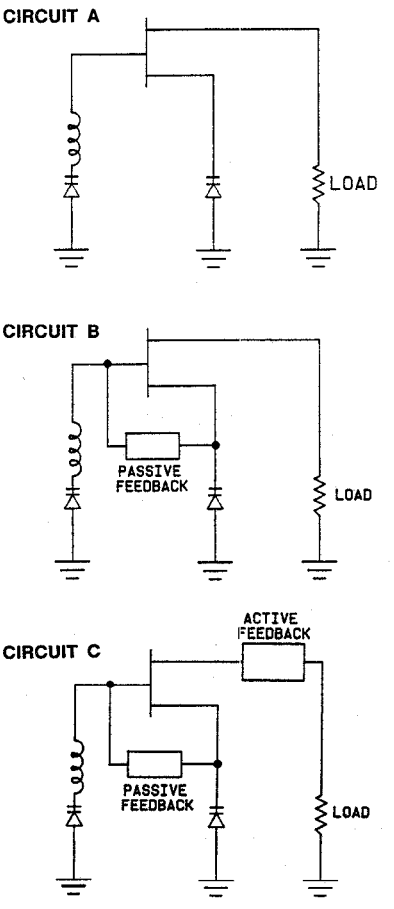

Figure 2. Three VCO Types.

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The drawback with the first two types (A, B) is that broad bandwidth is only achievable by presenting less than 5 ohms on the drain of the FET. The necessity of a low impedance load makes it difficult to tap the output of the oscillator. Other points of the circuit may be tapped for output but further analysis has shown that a load at any point other than the drain results in narrower bandwidth and poor load isolation. Thus the best choice is circuit C which can be loaded into a much higher impedance, such as 50 ohms, without sacrificing bandwidth.

Circuit C was optimized for maximum bandwidth using a 0.2 to 3 pF varactor in the gate and a 0.5 to 3 pF varactor in the source such that both varactors would be controlled by one tuning voltage. A single-ended buffer amplifier was cascaded to the drain of the oscillator so as to improve the load isolation and help stabilize the output power. The computer analysis indicates a tuning bandwidth of 85% with a tuning voltage from 0 to 25 volts. The analysis also predicted output power, harmonics, and modulation sensitivity which are summarized in Table 1. This topology is well suited for MMIC implementation which minimizes the parasitics so as to enhance the actual achievable bandwidth of the VCO.

EXPERIMENTAL RESULTS

MMIC Fabrication

The MMIC VCO was laid out and fabricated as a 32 x 48 mil die as shown in Figure 3. The active devices are 900um and 500um FETs with 0.5um gate lengths for the oscillator and the buffer amplifier, respectively. The FETs were actively biased in order to minimize the current consumption and improve the stability over temperature. On-chip DC filtering and AC coupling is achieved with MIM capacitors. All the bias points are on the MMIC chip so that the user need only provide one bias voltage.

The complete VCO circuit was hybridized by using chip varactors connected to the source and gate of the FET on MMIC as shown in Figure 4. The gate inductor was realized using one gold wirebond from the MMIC to the varactor. The gate varactor is a M/A-COM hyperabrupt GaAs varactor (0.2 to 3 pF) and the source varactor is an Alpha Industries hyperabrupt silicon varactor (0.5 to 3 pF). All of the elements are very small such that the entire circuit can be built into a 0.27" x 0.27" surface-mount package as shown in Figure 5.

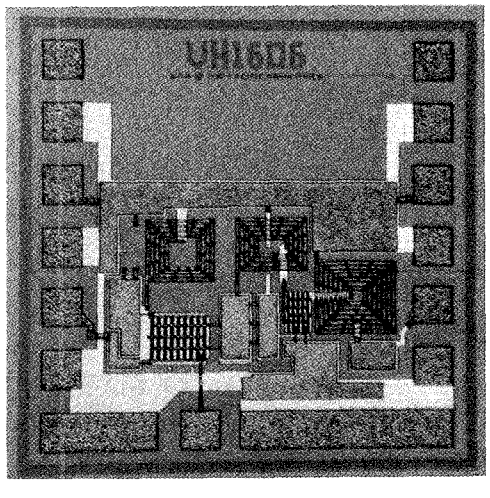

Figure 3. VCO Chip (32 x 48 mils).

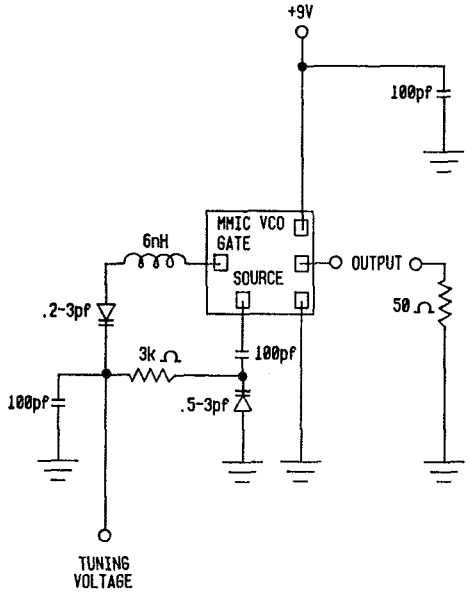

Figure 4. MMIC VCO Test Layout.

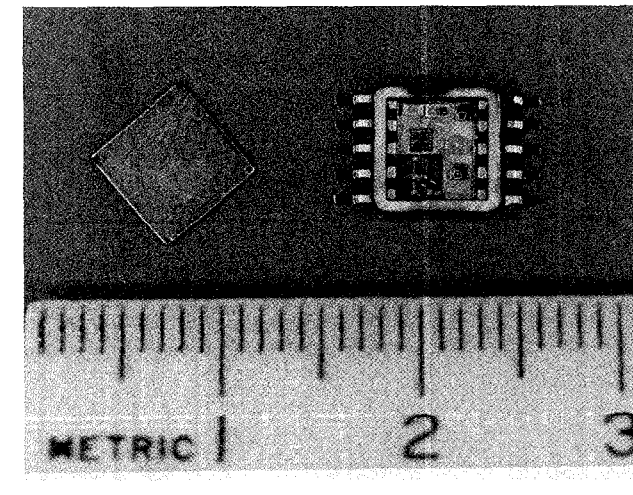

Figure 5. Photograph of MMIC in Ten-Lead Package.

Experimental Results

The MMIC VCO circuit was tested and achieved the predicted results. Table 1 is a summary of the test results compared with the predicted characteristics. The

circuit was also tested using a silicon varactor in the gate (identical to the source varactor).

Table 1. Predicted Characteristics and Test results of MMIC VCO

Parameter	Predicted	Measured
1. Operating voltage	6 to 10 V	5 to 10 V
2. Operating current	60 mA	55 mA
3. Usable frequency range	1.8 to 6.5 GHz	1.5 to 6.0 GHz
4. Tuning bandwidth		
with GaAs varactor:	85%	85%
with silicon varactor:	80%	78%
5. Output power	16.0 dBm	17.5 dBm
6. Phase noise @100 KHz		
with GaAs varactor:		<-92 dBc/Hz
with silicon varactor:		<-92 dBc/Hz
7. Harmonics	-20 dBc	-15 to -10 dBc
8. Modulation sensitivity		
with GaAs varactor:		68 to 230 MHz/volt
with silicon varactor:		52 to 230 MHz/volt
9. Linearity (frequency deviation from best fit straight line)		
with GaAs varactor:		±315 MHz
with silicon varactor:		±390 MHz
10. Post-tuning drift		
with GaAs varactor:		within 2 MHz in 1 msec
with silicon varactor:		within 2 MHz in 20 usec
11. Load pulling (into a 1.7:1 VSWR)		
low band:		11 MHz
high band:		20 MHz

Many of the above test results agree closely with the predicted values. The frequency range turned out to be shifted lower than predicted which is probably due to some stray capacitance associated with the varactor circuit. The tuning bandwidth of 85% is identical to the predicted value. A standard silicon hyperabrupt varactor was also used in the gate and the bandwidth decreased to about 78%. The tuning bandwidth window is easily selected by changing the length of the gate inductor wirebond. Bands covering 2.5 to 6.0 GHz and 1.5 to 4.0 GHz were achieved by changing the length of the gate wirebond.

The output power is higher than predicted because of the flexibility in selecting a bias voltage. Although as little as 5 volts can be used, the highest output power and best temperature characteristics are achieved using a 10 volt bias. At room temperature the output power is about 17.5 dBm with 10 volts and 60 mA and about 16.5 dBm with 5 volts and 60 mA with efficiencies of 9.3% and 15%, respectively. An output power spectrum is shown in Figure 6 indicating less than -92 dBc/Hz at a 100 KHz offset frequency.

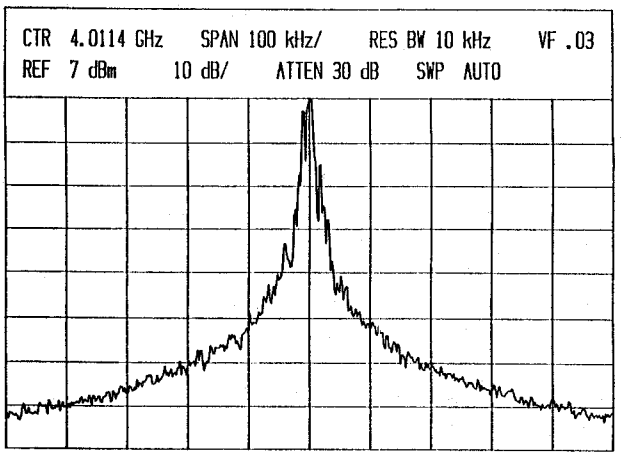

Figure 6. Output Spectrum of MMIC GaAs VCO.

The phase noise did not exceed -92 dBc/Hz at 100 KHz across the entire tuning bandwidth. This low phase noise is achievable because of the off-chip inductor and varactor tank circuit which have much higher Q than on-chip elements. The on-chip bias filtering also helps isolate the oscillator from bias line noise which also serves to improve the phase noise performance.

The harmonics rise to -10 dBc at the low end because they are still in the buffer amplifier gain band. The modulation sensitivity varies by about 4:1 with most of the variation at the high end of the band as shown in Figure 7. The large variation in modulation sensitivity is due to the combined non-linearity of the varactor tuning curve and the phase response of the MMIC circuit. The change in modulation sensitivity is only 7% over a selected tuning band of 2.5 to 4.0 GHz. The change in modulation sensitivity may be further improved over a wider band by utilizing various varactor reactance compensating techniques.

The linearity to a best fit straight line is ±315 MHz for the GaAs varactor and ±390 MHz for the silicon

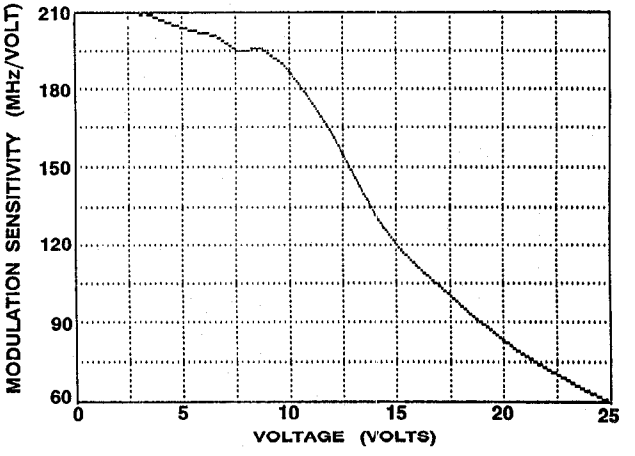

Figure 7. Modulation Sensitivity Variation Across the Tuning Bandwidth.

varactor. The linearity, just like the change in modulation sensitivity, is due to the inherent non-linearity of the varactor circuit and the MMIC. The linearity may also be improved by using varactor reactance compensation techniques.

The post tuning drift from low to high frequency was measured for both the GaAs and silicon varactors as shown in Figure 8. The curves indicate that the GaAs varactor is about 50 times slower than the silicon varactor to reach within 2 MHz of the final frequency. PTD is mainly influenced by the thermal time constant and the surface state of the varactor diode. The measured PTD values of 1 msec for GaAs and 20 usec for silicon are approximately the same as values commonly measured

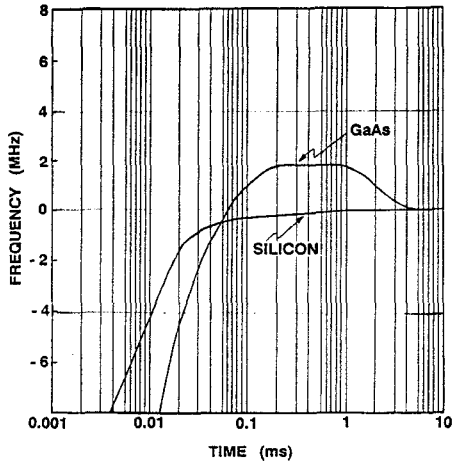

Figure 8. Post-Tuning Drift VCO with GaAs and Silicon Varactors.

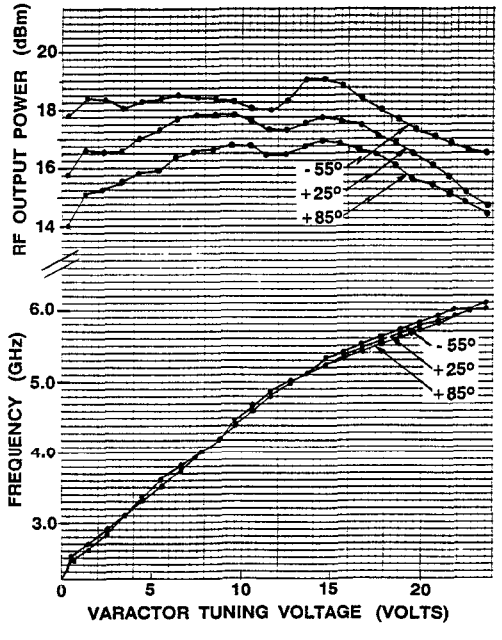

Figure 9. Output Power and Frequency vs. Tuning Voltage Over Temperature of VCO with GaAs Gate Varactor.

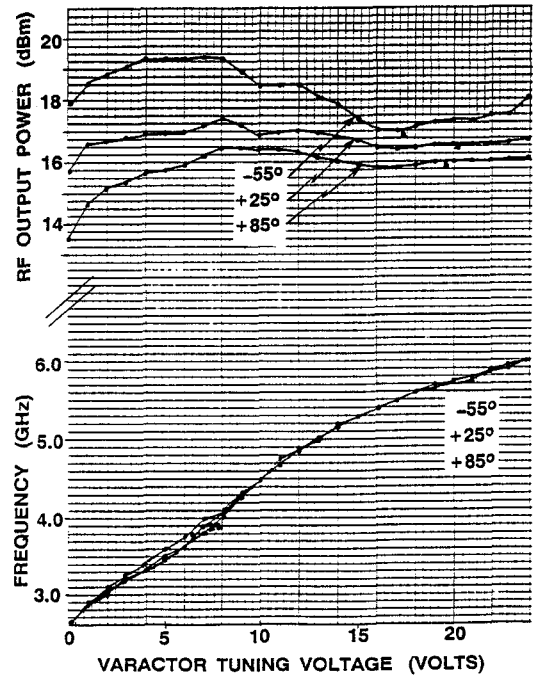

Figure 10. Output Power and Frequency vs. Tuning Voltage of VCO with a Silicon Gate Varactor.

for hybrid VCOs, which means that the MMIC device introduces no significant characteristics affecting tuning speed. The curves in Figures 9 and 10 show the frequency and output power characteristics over temperature for the gate GaAs varactor and gate silicon varactor, respectively.

The worst case frequency drift from -55 to +85 ^{o}C is about $\pm$150 MHz for both the GaAs varactor and the silicon varactor which is less than 9% of the total tuning bandwidth. The worst case power drift is about $\pm$1.5 dB from -55 to +85 ^{o}C.

CONCLUSION

A broadband MMIC VCO was successfully designed, fabricated and tested, tuning from 2.5 GHz to 6.0 GHz (85% bandwidth). Changing the tuning inductance allows band selection from 1.5 to 6.0 GHz. The circuit was designed by using both linear and non-linear computer aided design. The exceptional overall performance of the oscillator circuit and the small size make it versatile for commercial and military applications.

REFERENCES

1. Bently N. Scott, et al., "A Family of Four Monolithic VCO MIC's Covering 2-18 GHz," 1984 IEEE Monolithic Circuits Symposium Digest, pp. 58-61.

2. Sanjay B. Moghe and Thomas J. Holden, "High Performance MMIC Oscillators," IEEE MTTS, December 1987, pp. 1283-1287.